REMARKS

Applicants respectfully request reconsideration of the present application based on the foregoing amendments and the following remarks. Upon entry of the amendment, claims 1-6 and 8-64 will remain pending in the application.

Objections to Drawings

The examiner requested that formal drawings be submitted with a response to the Office Action, and Applicants are doing so concurrently with this Amendment.

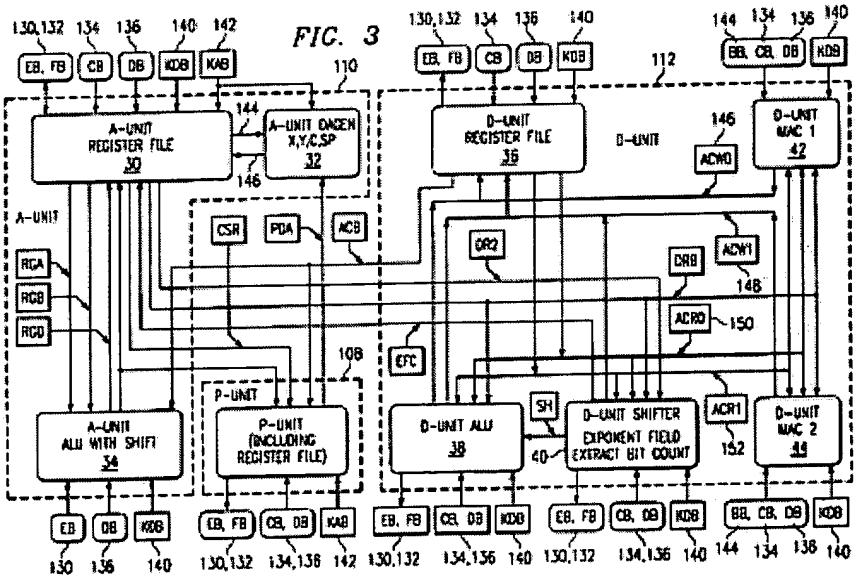
Claim Rejections Under 35 U.S.C. § 102(e)

The examiner rejected claims 1-6, 8-48 under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent No. 6,658,578 to Laurenti et al. ("Laurenti"). For reasons set forth more fully below, this rejection is respectfully traversed as to all claims.

What Laurenti Discloses

Laurenti discloses a programmable fixed point digital signal processor (DSP) with variable instruction length, whose architecture and instruction set are optimized for low power consumption and efficient execution of certain DSP algorithms. (col. 1, ll. 51-58). In one example implementation, the DSP is a processor core 102 provided in an ASIC.

FIG. 3



As shown in FIG. 3 of Laurenti (reproduced above), core 102 includes an Instruction Buffer Unit (I unit) 106, a Program Flow Unit (P unit) 108 that includes a register file, an Address Data Flow Unit (A unit) 110 having a register file 30, and a Data Computation Unit (D unit) 112 having a register file 36. (cols. 8 and 9). The A unit register file 30 includes 16 bit pointer registers AR0-AR7, data registers DR0-DR3, 16 bit circular buffer registers and 7 bit data page registers. The D unit register file 36 includes 40-bit accumulators AC0-AC3 and a 16 bit transition register.

Laurenti Does Not Disclose Any Hardware or Software Generation Means at All

Importantly in connection with the present invention, Laurenti discloses a completed microprocessor core architecture. Laurenti also discloses debugging and emulation facilities. (col. 8, lines 13-14). However, Laurenti does not disclose any means for generating a hardware description of the microprocessor core, apart from vaguely mentioning that it may be implemented in an ASIC. Laurenti simply does not disclose or suggest any means for configuring a processor, much less generating hardware and software based on that configuration.

Meanwhile, each of the independent claims 1, 39, 45 and 48 requires means for generating a hardware description of the processor based on a configuration specification, and a means for generating a software development tools for the hardware implementation based on a configuration specification. For at least this reason, the rejection of these independent claims, as well as all claims dependent therefrom, based on Laurenti is misplaced, and should be withdrawn.

Independent Claim 1 Patentably Defines Over Laurenti

Independent claim 1 requires, *inter alia*,

> hardware generation means for, **based on a configuration specification including a predetermined portion and a user-defined portion**, generating a description of a hardware implementation of the processor, the predetermined portion specifying a configuration of a core register file, and **the user-defined portion specifying whether to include a user-defined register file in the processor in addition to the core register file**;
>
> ...
>
> wherein the hardware generation means includes register generation means for, **based on the user-defined portion of the configuration**

specification, generating a description of the user-defined register file separate from and in addition to a description of the core register file in the description of the hardware implementation of the processor; and

The language of claim 1 thus explicitly requires that: (1) the **user-defined portion of the configuration specification** includes the ability to specify **whether a user-defined register file** should be included in the processor **in addition to** the core register file; and (2) the hardware generation means must be able to generate a description of a user-defined register file **separate from and in addition** to a description of the core register file in the description of the hardware implementation of the processor.

Laurenti discloses nothing about generating a hardware description of a processor, much less one having the configuration abilities described above, in which a user-defined register file may be optionally included in the processor hardware description.

The Office Action relies on this passage of Laurenti (col. 16, 63-66) as allegedly describing the claimed configuration specification and hardware generation means:

> The A-Unit ALU operator: It is used to make generic computation within the A-unit. Following instruction example uses this operator to add 2 A-unit register contents.
> AR1=AR1+DR1

This passage merely describes an example use of instruction operands in a completed processor having an architecture described by Laurenti's patent. Applicants respectfully submit that this passage says nothing about a configuration specification or a hardware generation means at all, much less the elements as claimed in claim 1.

The Office Action also relies on this passage of Laurenti (col. 44, lines 46-56):

> The instruction that will control this execution will offer dual addressing on the D and C buses as well as all possible combinations for the pair of operations among MPY, MPYSU, MAC and MAS operations and signed or unsigned operations. Destinations (Accumulators) in the Data Registers can be set separately per operation but accumulators sources and destinations are equal. Rounding is common to both operations. CFP pointer update mechanism will include increment or not of the previous value and modulo operation. Finally, Table 17, on next page, shows

application of the scheme depicted in FIG. 30 to different algorithms and RAM storage organization.

This passage merely describes an example use of instruction operands in a completed processor having an architecture described by Laurenti's patent. Applicants respectfully submit that this passage says nothing about a configuration specification or a hardware generation means at all, much less the elements as claimed in claim 1.

For at least these additional reasons, independent claim 1, together with rejected claims 2-38 that depend therefrom, patentably defines over the prior art and the § 102 rejection of the claims should be withdrawn.

Independent Claim 39 Patentably Defines Over Laurenti

Independent claim 39 requires, *inter alia*,

> hardware generation means for, **based on a configuration specification** including a predetermined portion and a user-defined portion, generating a description of a hardware implementation of the processor;
>
> . . .
>
> wherein the **configuration specification includes a statement specifying scheduling information of instructions** used in the software development tools;
>
> the hardware generation means is for, **based on the statement in the configuration specification, determining whether and how to generate a description** of at least one of pipeline logic, pipeline stalling logic and instruction rescheduling logic

The language of claim 39 thus explicitly requires that: (1) the **configuration specification** includes the ability to specify **scheduling information of instructions**; and (2) the hardware generation means must be able to determine **whether and how** to generate a description of instruction scheduling logic in the description of the hardware implementation of the processor based on the instruction scheduling information in the configuration specification.

Laurenti discloses nothing about generating a hardware description of a processor, much less one having the configuration abilities described above, in which certain types of instruction scheduling logic may be optionally included in the processor hardware description.

The Office Action relies on this passage of Laurenti (col. 6, lines 53-56) as allegedly describing the claimed configuration specification and hardware generation means:

> FIG. 128 is a timing diagram of the pipeline illustrating a current instruction scheduling a CPU resource update conflicting with an update scheduled by an earlier instruction;

This passage merely indicates that Laurenti's processor includes instruction scheduling logic. Applicants respectfully submit that this passage says nothing about a configuration specification or a hardware generation means at all, much less the elements as claimed in claim 39.

The Office Action also relies on this passage of Laurenti (col. 33, lines 46-48):

> Each READY line associated to a memory request is monitored at CPU level. In case of not READY, it will generate a pipeline stall.

This passage merely describes an example pipeline stall operation in a completed processor having an architecture described by Laurenti's patent. Applicants respectfully submit that this passage says nothing about a configuration specification or a hardware generation means at all, much less the elements as claimed in claim 39.

For at least these additional reasons, independent claim 39, together with rejected claims 40-48 and 58-60 that depend therefrom, patentably defines over the prior art and the § 102 rejection of the claims should be withdrawn.

Independent Claim 45 Patentably Defines Over Laurenti

Independent claim 45 requires, *inter alia*,

> **document generation means for generating documentation of a processor instruction set** described by the configuration specification **based on the configuration specification**.

Laurenti discloses nothing about generating a document generation means, much less one that generates documents based on a configuration specification as required by claim 45. The

Office Action correctly fails to point to any description in Laurenti corresponding to this subject matter.

For at least these additional reasons, independent claim 45, together with rejected claims 46-47 and 61-62 that depend therefrom, patentably defines over the prior art and the § 102 rejection of the claims should be withdrawn.

Independent Claim 48 Patentably Defines Over Laurenti

Independent claim 48 requires, *inter alia*,

> hardware generation means for, **based on a configuration specification** including a predetermined portion and a user-defined portion, **generating a description of a hardware implementation of the processor**; and
>
> . . .
>
> wherein the user-defined portion of **the configuration specification includes a user-defined specification of a processor exception and when a processor instruction raises the exception**; and
>
> the hardware generation means **includes user-defined exception support generating means for generating hardware supporting that user-defined exception** as part of the processor hardware implementation.

The language of claim 48 thus explicitly requires that: (1) the **configuration specification** includes the ability to optionally include **user-defined processor instruction exceptions**; and (2) the hardware generation means must be able to **generate hardware supporting the user-defined exception** in the description of the hardware implementation of the processor based on the configuration specification.

Laurenti discloses nothing about generating a hardware description of a processor, much less one having the configuration abilities described above, in which user-defined processor instruction exceptions may be optionally included in the processor hardware description.

The Office Action relies on this passage of Laurenti (col. 35, lines 44-57) as allegedly describing the claimed configuration specification and hardware generation means:

> FIG. 27 describes the formats for all the various data types of processor 100. The DU supports both 32 and 16 bit arithmetic with proper handling of overflow exception cases and Boolean variables. Numbers representations include signed and unsigned types for all arithmetic.

> Signed or unsigned modes are handled by a sign extension control flag called SXMD or by the instruction directly. Moreover, signed values can be represented in fractional mode (FRACT). Internal Data Registers will include 8 guard bits for full precision 32-bit computations. Dual 16-bit mode operations will also be supported on the ALU, on signed operands. In this case, the guard bits are attached to second operation and contain resulting sign extension.

This passage merely indicates that Laurenti's processor includes support for overflow exceptions. Applicants respectfully submit that this passage says nothing about a configuration specification or a hardware generation means at all, much less the elements as claimed in claim 48 in which hardware is generated in support of a user-defined processor instruction exception.

For at least these additional reasons, independent claim 48, together with rejected claims 63-64 that depend therefrom, patentably defines over the prior art and the § 102 rejection of the claims should be withdrawn.

Independent Claim 49 Patentably Defines Over Laurenti

Independent claim 49 requires, *inter alia*,

> hardware simulation means for executing a hardware description of an extensible processor;
> software simulation means for executing a software reference model of the extensible processor; and
> **cosimulation means for operating the hardware simulation means and the software simulation means** and comparing results of simulations therefrom to **establish correspondence between the hardware description of the extensible processor and the software reference model of the extensible processor**.

Laurenti discloses nothing about cosimulation means that operates a hardware simulation means and software simulation means, much less one that establishes correspondence between the hardware description and the software reference model as required by claim 49.

The Office Action relies on this passage of Laurenti (col. 161, lines 26-34) as allegedly describing the claimed cosimulation means:

> A Cache will improve the overall performance of a system because of the program locality or locality of reference principle. No Cache will work if the program accesses memory in a completely random fashion. To evaluate the architecture of a Cache, it is necessary to do statistical optimisations. A Cache architecture may be very good for a given program, but very bad for a different program. Hence it is very important to perform simulations and measure the performance on the actual prototypes.

This passage merely indicates that simulations can be performed to measure performance of possible caches for use with prototypes of Laurenti's processor. Applicants respectfully submit that this passage says nothing about a hardware and software cosimulation means at all, much less the one required in claim 49.

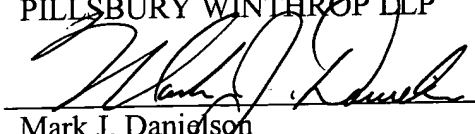
For at least these additional reasons, independent claim 49, together with rejected claims 50-57 that depend therefrom, patentably defines over the prior art and the § 102 rejection of the claims should be withdrawn.

Conclusion

All objections and rejections having been addressed, it is believed the present application is in condition for allowance, and Notice thereof is earnestly solicited. If any issues remain which the Examiner feels may be resolved through a telephone interview, s/he is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,
PILLSBURY WINTHROP LLP

Date: October 4, 2004



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